Hybrid Spintronics-Straintroncis: An ultra-energy efficient approach to nanomagnetic memory and logic

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We have theoretically shown that flipping the magnetization of "multiferroic" nanomagnets, consisting of a magnetostrictive layer and a piezoelectric layer, with a tiny voltage applied across the piezoelectric layer that generates strain the magnetostrictive layer, is extremely energy-efficient and dissipates less than 1 atto-Joule (aJ) of energy at a clock rate of ~ 1 GHz [1, 2, 3, 4]. That makes such "switches" potentially ~1000 times more energy efficient than CMOS switches in digital logic and memory.

In this talk, we will describe strain-mediated Bennett clocking of dipole-coupled nanomagnet arrays for propagating logic bits [1], writing of bits in magnetic memory with strain and associated energy dissipation [2,3], design of universal multiferroic logic gates that perform logic operations while dissipating only ~ 2 aJ of energy per bit flip at ~1 GHz sinusoidal clock rate [4,5], 4-state logic [6] and image processing implemented with arrays of nanomagnets that can reconstruct a 512×512 pixel noise-corrupted grayscale image in ~ 2 ns [7].

One key issue in using an architecture that utilizes dipole coupling between nanomagnets in implementing logic functionality is that the reliability of switching can be low if (i) dipole coupling is not sufficient or (ii) the stress/strain application and withdrawal process makes it easy for thermal noise to "kick" the magnetization into an unfavorable orientation during switching. In the latter half of the talk we will present our preliminary findings on these issues. Ultimately, the need to understand these issues better could motivate experiments to study nanoscale magnetization dynamics with sub-nanosecond resolution at the ALS.

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